ELEC50001 EE2 Circuits and Systems

Problem Sheet 5 Solutions – Data Converters (*Lectures 10 and 13*)

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. Full-scale range = 3998 so the accuracy is 2/3998 of full-scale range. For an N-bit binary A/D converter, the full-scale range is $(2^N–1)$ LSB giving an accuracy of $0.5/(2^N–1)$.

Hence $\frac{0.5}{2^N-1} \le \frac{2}{3998} \quad \Rightarrow \quad 2^N \ge 1000.5 \quad \Rightarrow \quad N \ge 9.96 \quad \Rightarrow \quad N = 10$

2B. –2047 mV ±0.5 mV, i.e. –2047.5 mV to –2046.5 mV.

3B. 1 V and 8 V correspond to output values of 100 and 800 respectively, so if 1 V < x < 8 V, the output will be in the range 100 to 799.

4C. A change of 5 V in V3 must give a change of –1 V in VOUT, a gain of –0.2. Hence RF/R3 = 0.2 ⇒ R3 = 50 kΩ.

When V3=0, the op-amp may be viewed an a non-inverting amplifier with a gain of (1 + RF/R3) = 1.2. The voltage at VOUT due to V2:0 is therefore given by:

$$V_{OUT} = 1.2 \times \frac{G_2V_2 + G_1V_1 + G_0V_0}{G_4 + G_2 + G_1 + G_0}$$

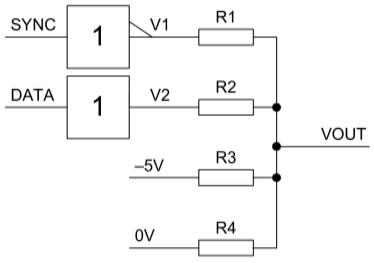
where G4:0 are the reciprocals of R4:0.

To minimize the effect of op-amp bias currents, we should make the Thévenin impedances at the input terminals equal. This means that G4+G2+G1+G0 = G3+GF = 120 μS.

The gains from V2, V1 and V0 to VOUT must be 0.1, 0.05 and 0.025 respectively. Thus we have G2 = 120 μS × 0.1/1.2 = 10 μS ⇒ R2 = 100 kΩ. Similarly, R1 = 200 kΩ and R0 = 400 kΩ.

Finally G4 = 120 μS – G2 – G1 – G0 = 102.5 μS ⇒ R4 = 9.8 kΩ.

5C. The SYNC signal needs inverting because SYNC going high must cause the output to decrease. We will need a negative bias voltage in order to obtain –0.3 V. Our circuit is therefore:



Taking Gn = 1/Rn we must have G1+G2+G3+G4 = 1/50Ω = 20 mS.

Then VOUT = $(V_1G_1 + V_2G_2 – 5G_3) / 20$ mS.

From the truth table, we see that changes of 5 V in V1 and V2 must give changes in VOUT of 0.3 and 0.7 volts respectively; this means we need gains of 0.06 and 0.14. Hence:

G1 = 0.06 × 20 mS = 1.2 mS ⇒ R1 = 833Ω.
G2 = 0.14 × 20 mS = 2.8 mS ⇒ R2 = 357Ω.
To generate the –0.3 V offset: 5G3 = 0.3 × 20 mS = 6 mS ⇒ R3 = 833Ω.
G4 = 20 mS – G1 – G2 – G3 = 14.8 mS ⇒ R4 = 67.6Ω.

Note it is possible to take R4 to +5 V instead in which case R3 and R4 are 116Ω and 135Ω.

This circuit is very fast since it has no op-amps.

6B. The range of a 16-bit signed number is ±32767 and so to avoid distortion, the RMS value must be no higher than 3276.7. From the notes, the RMS value of quantisation noise is 0.289 LSB which gives a signal-to-noise ratio of 11338 which equals 81 dB

7C. Full-scale range of 20 V equals 4096 LSB so 0.5 LSB = 0.5 × 20/4096 = 2.44 mV.

The peak rate of change of a 10 V sinewave is $20\pi f$ volts per second. The voltage change in 5 ns is therefore $\pi f \times 10^{-7}$. These are equal when $f = 2.44 \times 10^{-3} \times 10^{7} / \pi = 7.77$ kHz.

For the second part $I = C\,dV/dt$ from which $\Delta t = C \times \Delta V / I = 2 \times 10^{-10} \times 2.44 \times 10^{-3} / 10^{-9} = 488$ μs.